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METHOD FOR PACKING SEMICONDUCTOR ELEMENTS

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[There are no amendments to this patent.]

Abstract

Objective

To reduce the functional test in a semiconductor element unit and the packing area of the semiconductor element.

Constitution

A solder bump 4 is formed on each connecting pad of a pair of semiconductor elements 3 that are functionally mutually dependent and opposite. A TAB inner lead 5 connected to a TAB lead frame 7 is connected between the semiconductor elements 3 so that it is sandwiched by the solder bumps 4. After the semiconductor elements 3 are connected and subjected to a functional test, a TAB outer lead 6 is connected to the TAB inner frame 7, and the TAB outer lead 6 is connected to a circuit conductor 2 of a circuit substrate 1.

Claims

1. A method for packing semiconductor elements characterized by the fact that it forms a solder bump on each

connecting pad of a pair of semiconductor elements, which are functionally mutually dependent and opposite, and connects the above-mentioned semiconductor elements in such a manner that an inner lead connected to a TAB lead frame is sandwiched by the above-mentioned solder bumps.

2. The method for packing semiconductor elements of Claim 1, characterized by the fact that it connects the above-mentioned semiconductor elements, completes its functional test, connects an outer lead to the above-mentioned TAB lead frame, and connects the outer lead to an external terminal of a circuit substrate for packing the above-mentioned semiconductor elements.

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